UNIT-2
Transistors

Syllabus

Bipolar Junction Transistor: Transistor Construction, Operation, Amplification action. Common Base, Common Emitter, Common Collector Configuration
Field Effect Transistor: Construction and Characteristic of JFETs. Transfer Characteristic. MOSFET (MOS)(Depletion and Enhancement) Type, Transfer Characteristic.

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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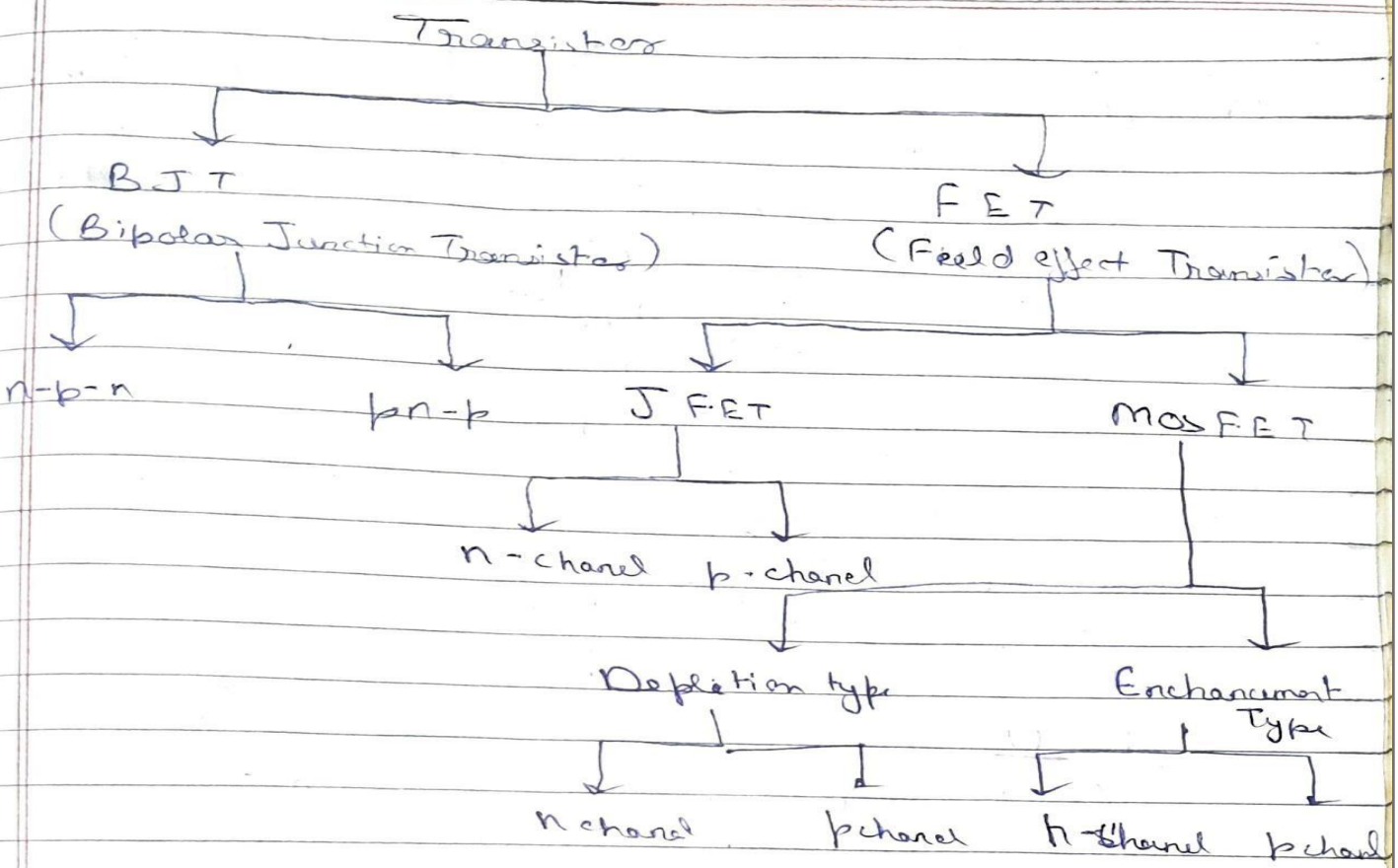
Unit 2



Transistor is a device which transfer applied signal from one type of resister to other type. e.g. signal can be transferred from low resistor to high or from high resistor to low resistor

Transistor (Transfer + resistor)

Transistor is called bipolar device because its operation depends on the interaction of majority and minority carriers both.

Construction of Transistor (BJT)

When in between two thick semiconductor a thin semiconductor is fused then arrangement is so formed is known as transistor

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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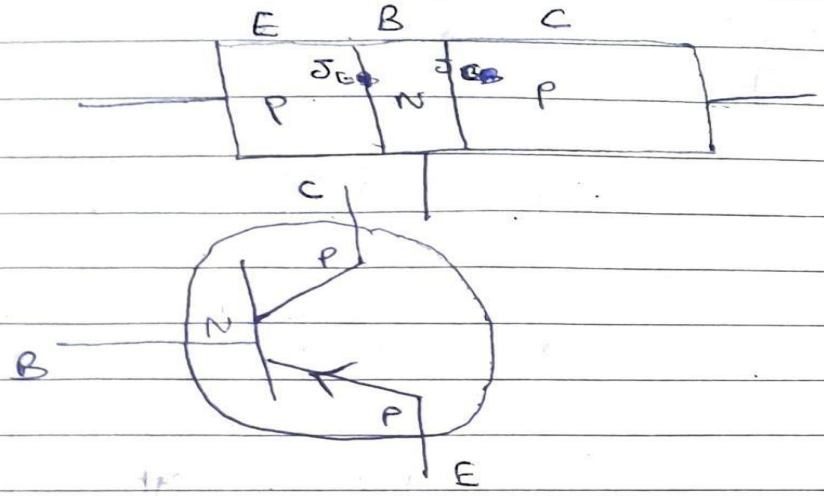
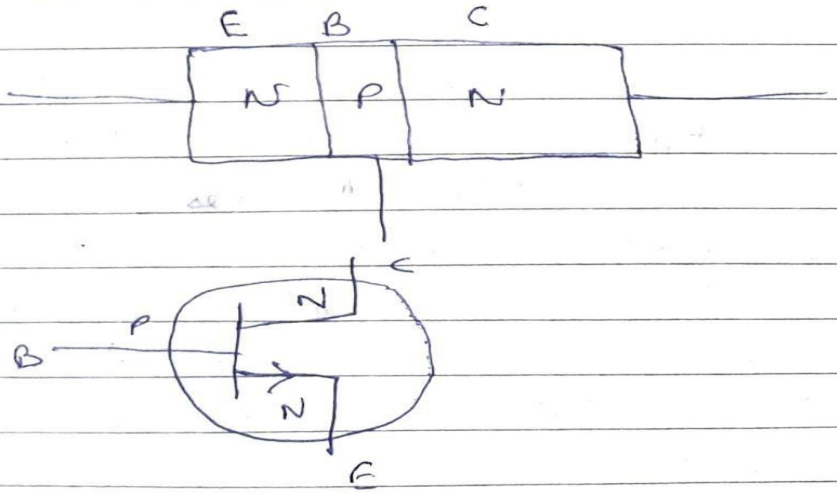
There are two type of transistor :.

(1) PNP Transistor When in between two thick p type semiconductor a thin n type semiconductor is fused then the transistor so formed is known as PNP Transistor



(2) NPN Transistor : When in b/w two thick n type s/c a thin p type s/c is fused then the transistor so formed is known as NPN Transistor



There are three main regions of transistor :.

(1) Emitter : . The region from which holes or e^- are emitted it is of moderate in size and heavily dopped

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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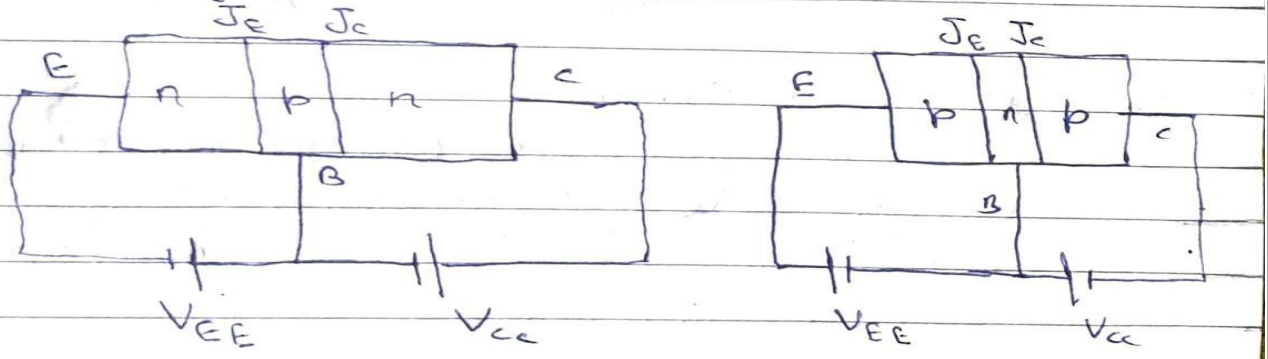
② **Base**: The middle layer of the transistor is called called Base It is very thin and lightly dopped.

③ **Collector**: The region which collects the the holes or e^- emitted from emitter is called collectors. It is large in size and moderately dopped..

Size $C > E > B$
dopping $E > C > B$

Mode of Operations

① • **Active Mode or region**:-
In active region emitter-base junction (JE) is forward biased and collector-base junction (J_c) is reverse biased. In this region transistor works as an amplifier



② ~~In this regi~~: **Saturation region**:
In this region emitter-base junction (JE) and collector base junction (JC) are forward biased. In this region transistor works as a closed switch

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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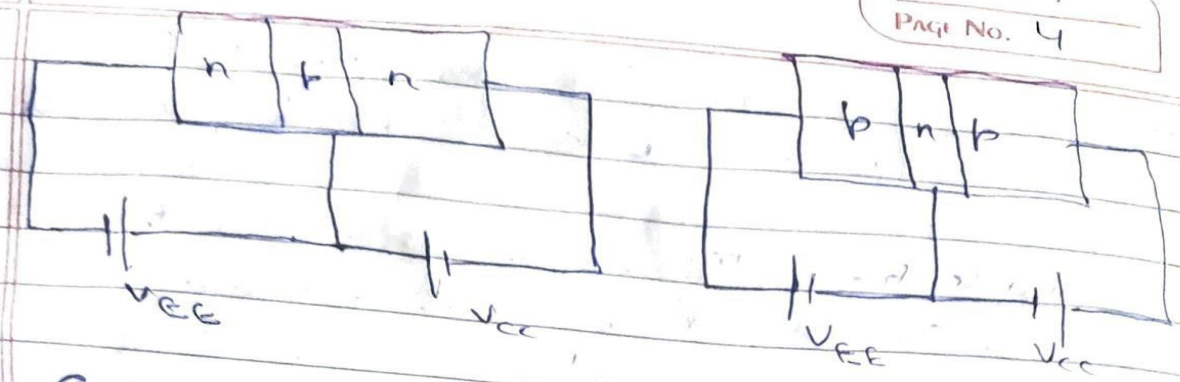
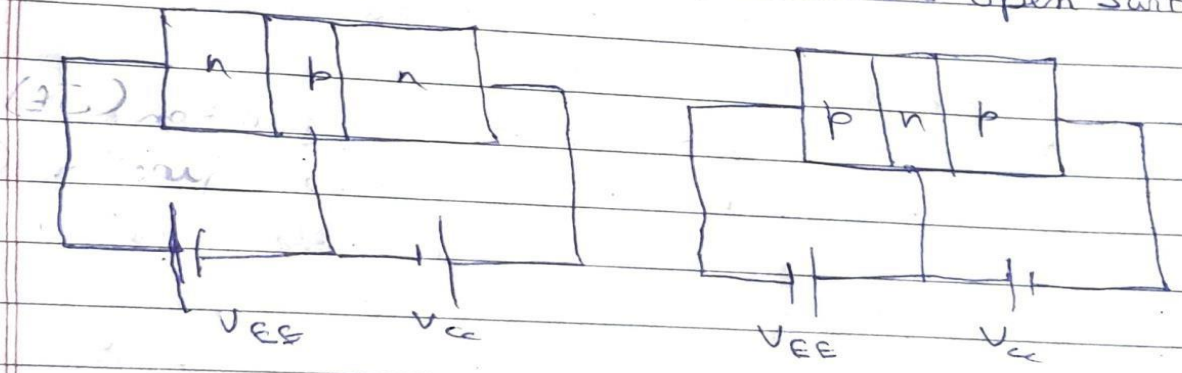


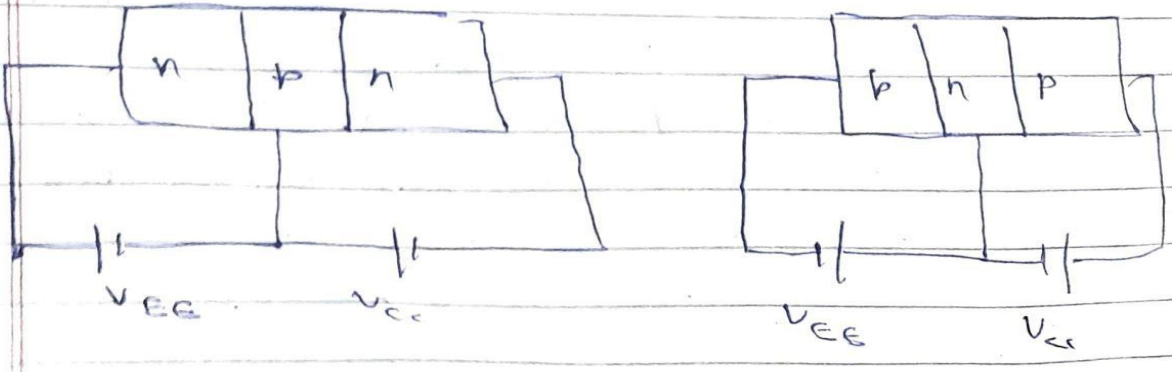
(3) **Cut-off region:-**

In this region emitter-base junction (J_E) and collector base junction (J_C) are reverse biased. In this region transistor work as a open switch.



(4) **Reverse Active mode:-**

In this region emitter Base junction (J_E) is reverse biased while collector base Junction is forward biased. In this region transistor never operated because current gain is negligible.



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+91-7088171324
Agrawalvedansh1999@gmail.com

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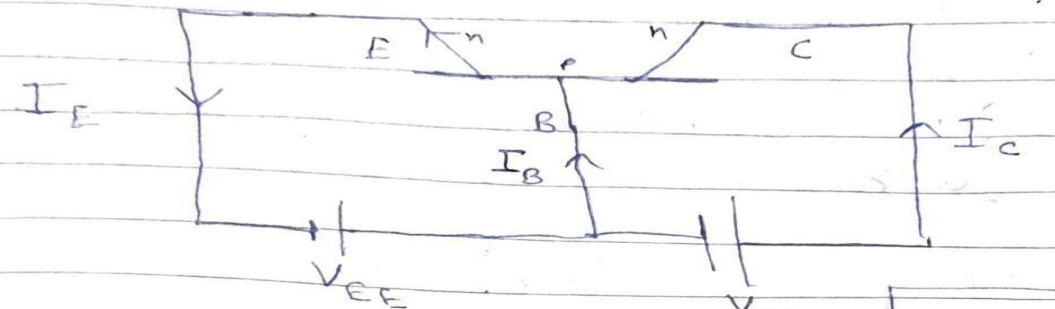
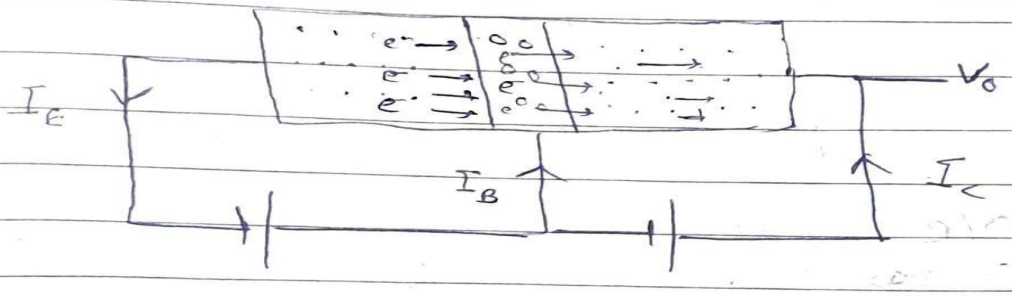
Common base Configuration



$$I_E = I_B + I_C$$



e^- from the emitter region are repelled by -ve terminal of the battery V_{EE} giving the emitter current I_E 5-7% of e^- get combine in the base with the holes giving the base current and remaing 95 % will move to collector giving collector current

Current gain :- It is a ratio of o/p current and i/p current

$$\alpha = \frac{I_c}{I_E}$$

Voltage gain :

$$A_V = \frac{I_c R_c}{I_E R_E} = \alpha \frac{R_c}{R_E}$$

Power gain :

$$P_G = VI \Rightarrow \alpha \frac{R_c}{R_E} \times \frac{I_c}{I_E}$$

$$P_G = \alpha^2 \frac{R_c}{R_E}$$

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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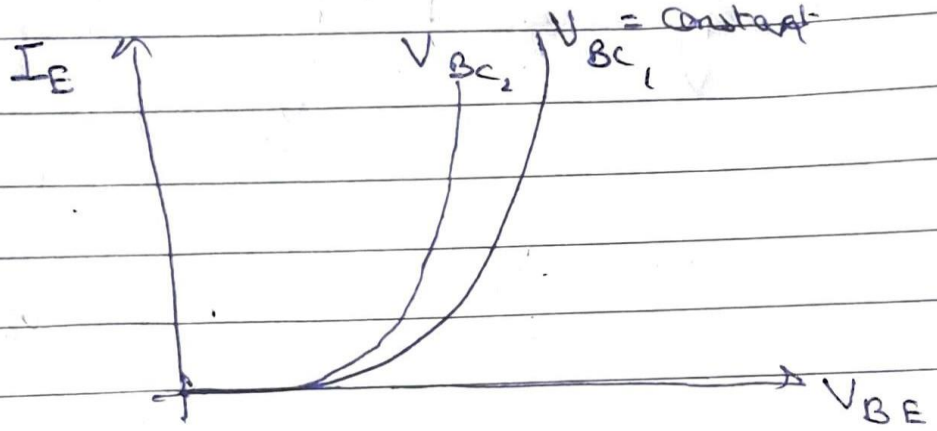
I/p O/p characteristics of CB configuration

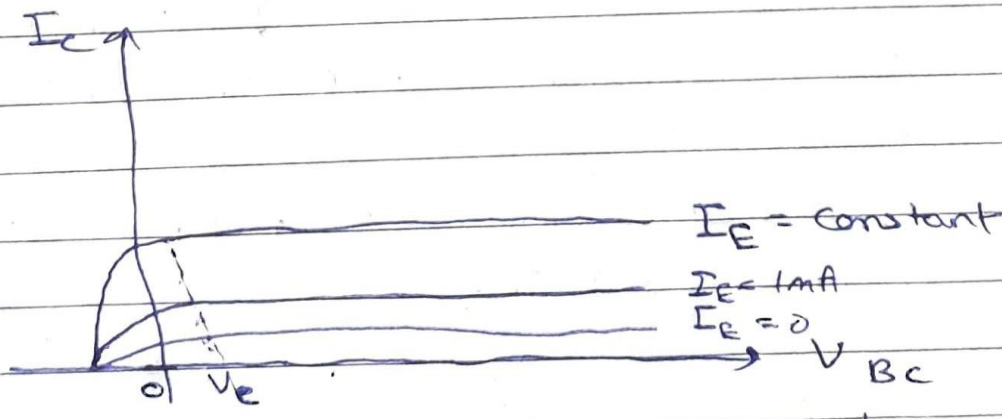
→ **I/p characterstics :-**

~~It is a curve b/w~~ The variation in the emitter current (I_E) with respect to change in base to emitter voltage V_{BE} at constant collector to base voltage V_{BC}



→ **O/p characterstics :-**

The variation in the collector current(I_C) with change in collector to base voltage V_{BC} at constant emitter current (I_E)



in which become

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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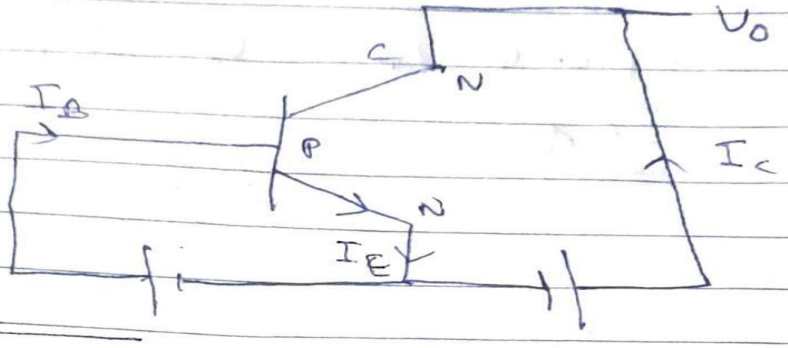
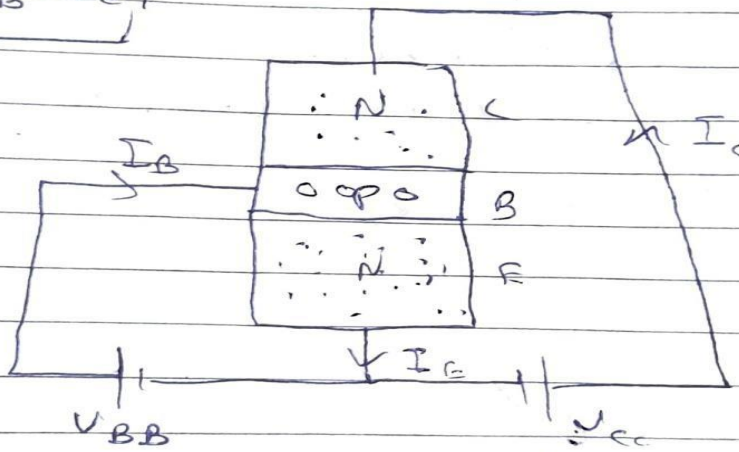
Common Emitter configuration



$$I_E = I_B + I_C$$



The emitter e⁻'s are repelled by -ve terminal of the battery V_{BB} giving emitter current (I_E). 5% of e⁻ get combined with holes in the base region giving the base current and remaing 95% will more to collector giving the collecter current

Current gain

$$\beta = \frac{I_C}{I_B}$$

$$\text{Voltage gain} = \beta \frac{R_C}{R_B}$$

$$\text{Power gain} = \beta^2 \frac{R_C}{R_B}$$

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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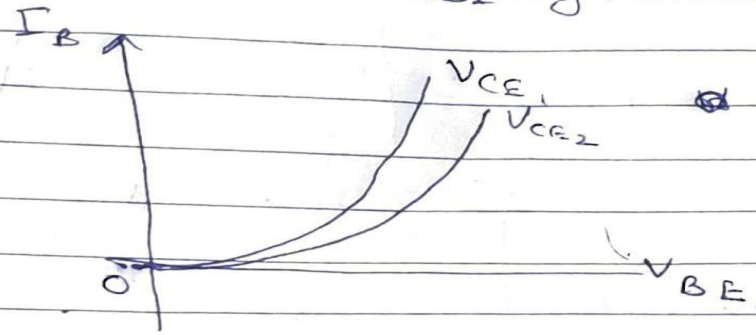
I/P O/P Characteristics of CE configuration

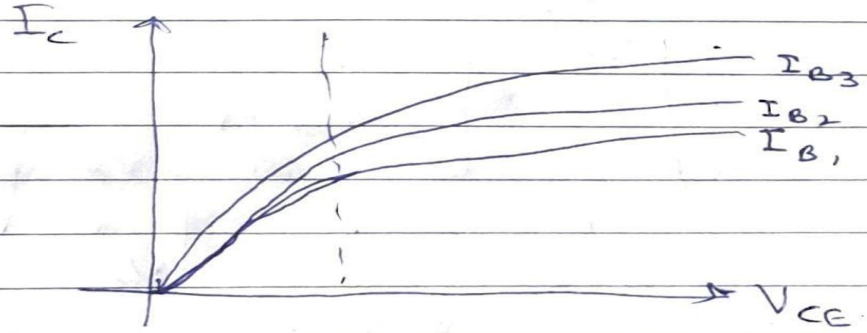
I/P characteristics :-

It is a plot of I_B and V_{BE} by maintaining V_{CE} constant

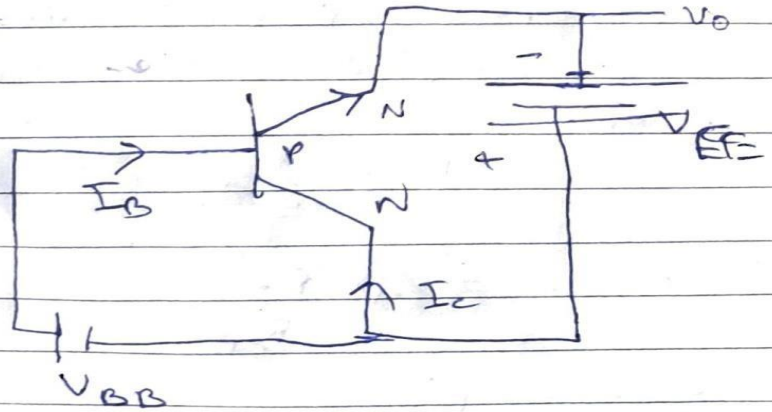


O/P characteristics :-

A plot of I_c and V_{CE} while maintaing I_B constant



Common Collector Configuration



Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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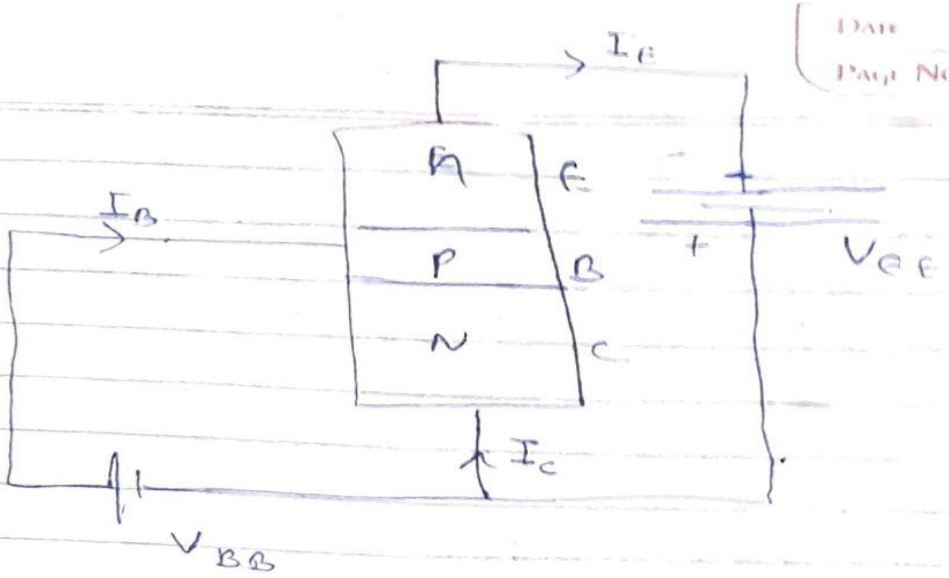


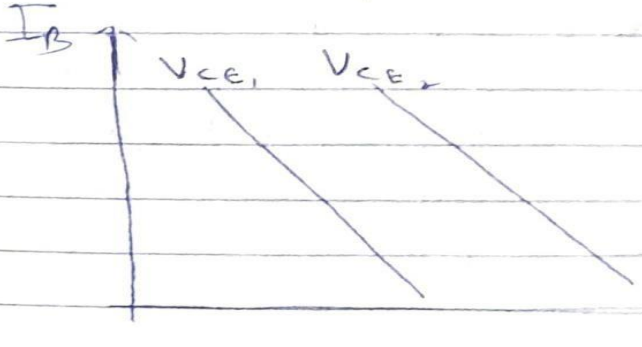
emitter emitter e^- giving I_E at Base 5% of e^- are recombine giving I_B and remaining 95% of e^- move to collector giving I_C

$$\gamma = \frac{I_C}{I_B}$$

I/P O/P characteristics of CC configuration

I/P characteristics:-

It is a plot of I_B and V_{CB} by maintaining V_{CE} constant



$$V_{BE} + V_{EB} = V_{EC}$$
$$V_{BE} = V_{CE} - V_{CB}$$

O/P characteristics:-

It is a plot of I_E and V_{EC} by maintaining I_B constant

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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Relationship b/w α, β and γ

We know $I_E = I_B + I_C$

Dividing by I_C

$$\frac{I_E}{I_C} = \frac{I_B}{I_C} + \frac{I_C}{I_C}$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

Now $(1+\beta)\alpha = \beta$

$\alpha + \alpha\beta = \beta$

$\alpha = \beta - \alpha\beta$

$\alpha = \beta(1-\alpha)$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

Again

$I_E = I_B + I_C$

Dividing by I_B

$$\frac{I_E}{I_B} = 1 + \frac{I_C}{I_B}$$

$$\boxed{\gamma = 1 + \beta}$$

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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$$\gamma = \frac{1+\alpha}{1-\alpha}$$

$$\gamma = \frac{1-\alpha+\alpha}{1-\alpha} = \frac{1}{1-\alpha}$$

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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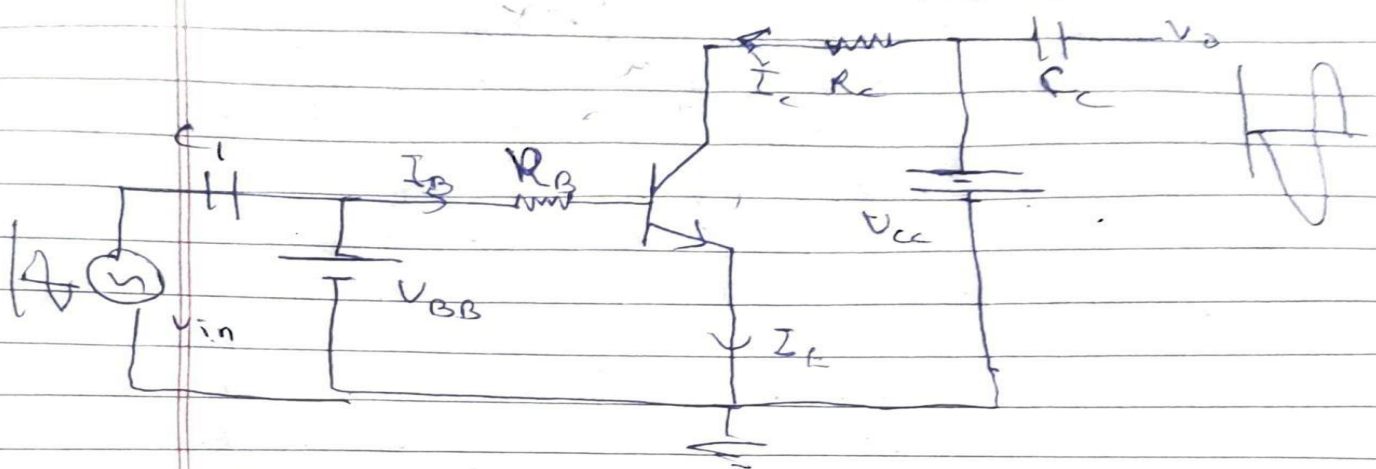
BJT As an Amplifier



When no i/p voltage is applied

$$I_E = I_B + I_c \quad \text{---(1)}$$

$$V_o = V_{cc} - I_c R_c \quad \text{---(2)}$$

Now i/p ac voltage to be amplified to the i/p emitter base circuit. When +ve half cycle of i/p ac signal comes it support the forward biasing of i/p emitter base circuit Due to it emitter current ↑es and collector current ↑ from eq(1) so V_o become less (from eq(2)) i.e. more -ve during +ve half cycle

When -ve half cycle of i/p ac voltage comes it oppose the forward biased of i/p emitter base ckt. Due to it emitter current ↓s and collector current ↓ therefore from eq(2) V_o become more +ve

Thus in CE amplifier ckt the i/p and o/p s/g voltage are in opposite phase

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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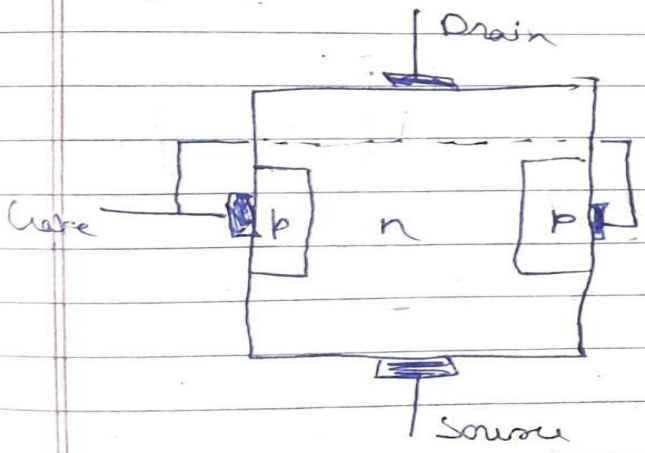
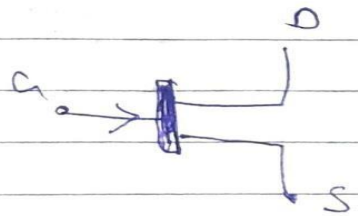
Field-effect Transistor (FET)

FET is a three terminal (namely drain, source and gate) s/c device in which current conduction is by only one type of majority carriers (e^- in n-channel or holes in p channel). It is also called unipolar Transistor

n-Channel JFET (Junction Field effect Transistor)

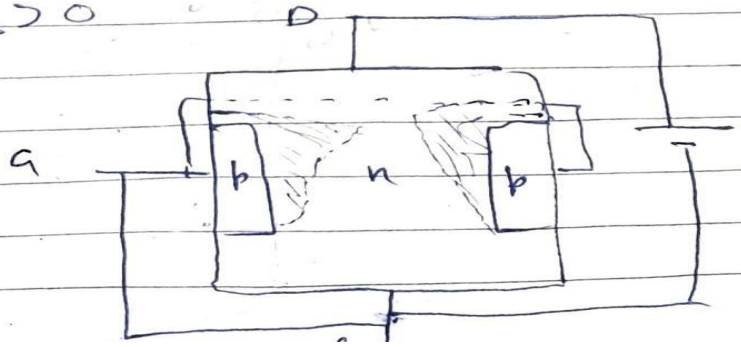
n channel JFET have n type base on both side of base two heavily doped p region are formed so two p-n junction is formed which are internally connected by a gate termind. Other Two terminal are drain and Sour





Working of n-Channel JFET

Case I $V_{GS} = 0$ $V_{DS} > 0$



Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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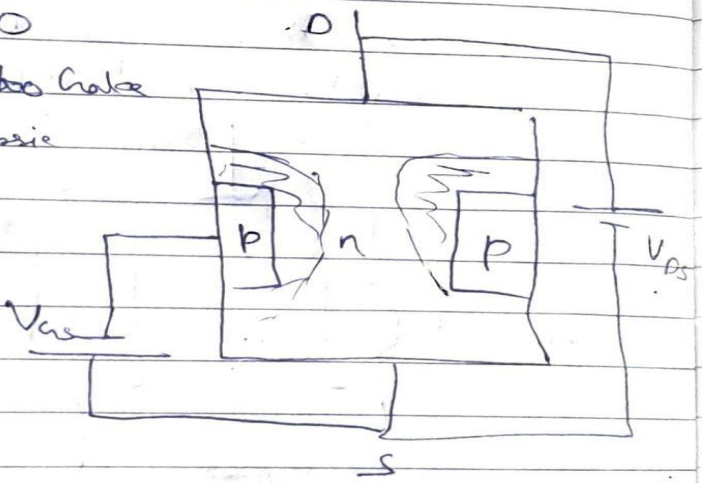
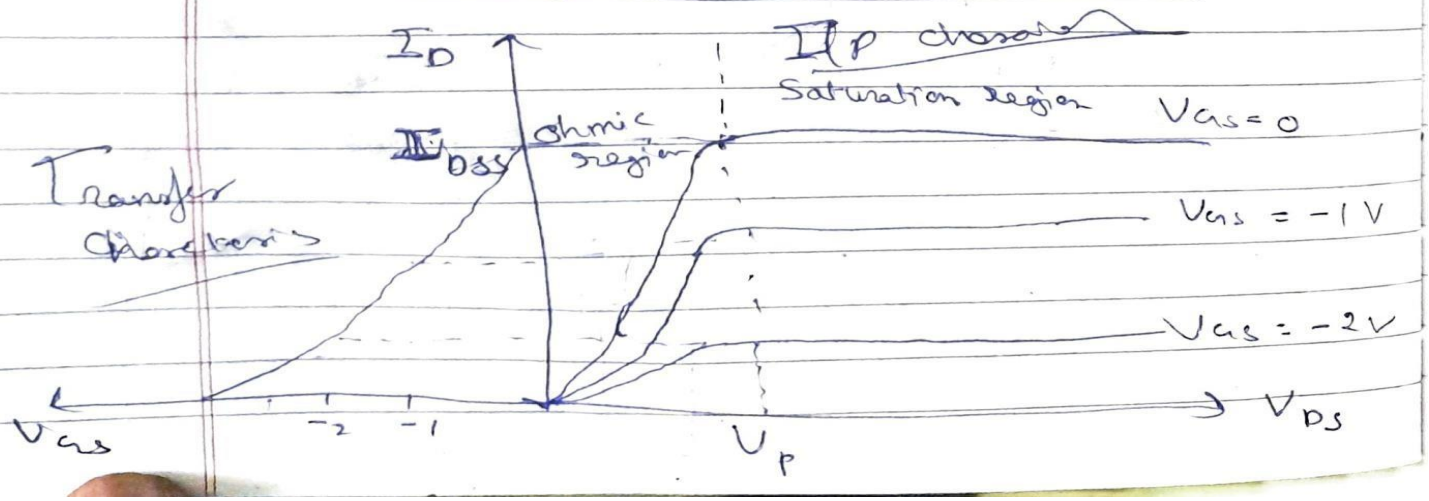
In JFET structure the channel is uniformly doped and If current flowing from drain to source the voltage of upper part of the channel is higher than the lower part so if $V_{DS} > 0$ and $V_{GS} = 0$ both pn junction are reverse biased ~~and~~ This reverse bias voltage is not uniform and decrease as we move downwards So a non uniform depletion region is formed at junction. At certain value of V_{DS} width of depletion layer becom max. and drain current become constant It is called pinch off voltage (V_P)

Case II $V_{DS} > 0$ $V_{GS} < 0$

In this case ~~sour~~ Gate junction become reverse biased so pinch off voltage get before Case I



Transfer characteristics of the JFET



Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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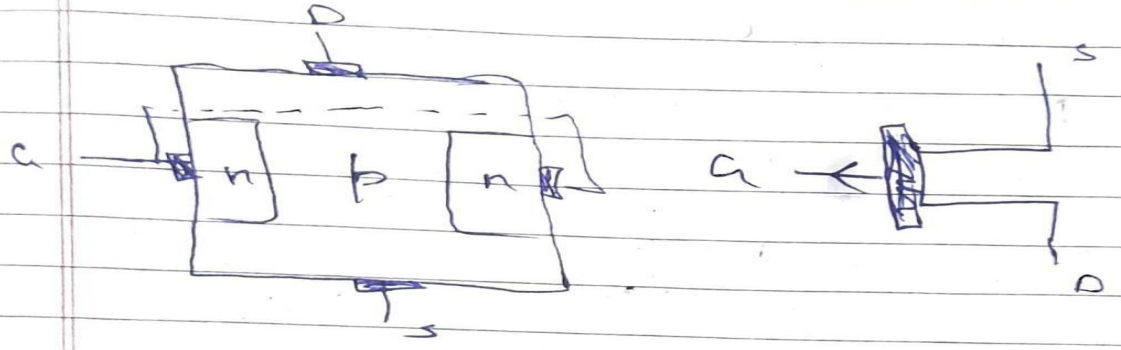
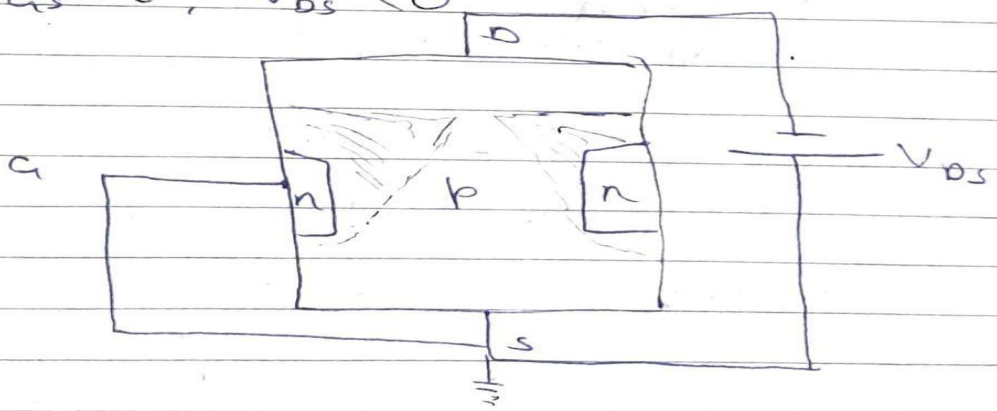
p channel JFET

In p channel JFET have p type base on both side of base two heavily dopped ~~p type~~ n region are formed so two pn junction is formed which are internally connected by gate and other two are drain and source



Working of p channel JFET

(case I) $V_{GS} = 0$, $V_{DS} < 0$



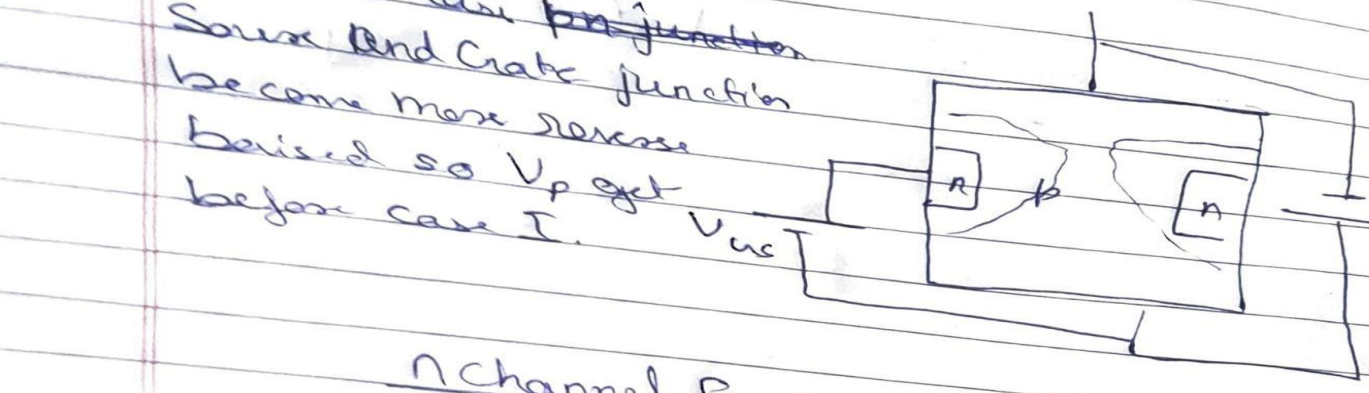
In JFET structure the channel is uniformly doped If current flowing from drain to source voltage of upper part of channel is lower than the lower part so if $V_{DS} < 0$ and $V_{GS} = 0$ both pn junction are reverse biased. This reverse bias voltage is not uniform and ↓ as we move downwards so a non uniform depletion region is formed at junctions.

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

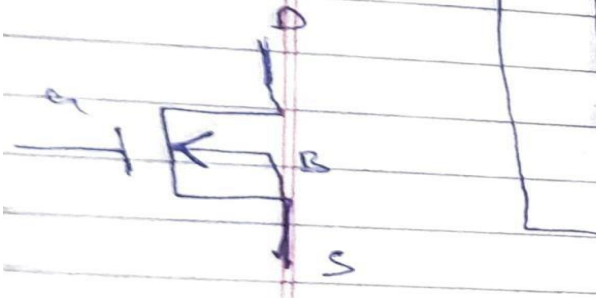
At certian value V_{DS} width of depletion region becom max. and drain current become constant

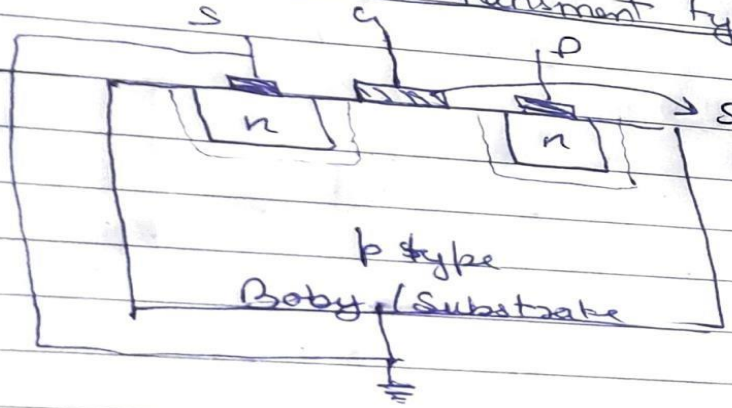
Case II) $V_{GS} > 0$ $V_{DS} < 0$

In this case ~~pn junction~~ Source and Gate junction become more reverse biased so V_p get befor case I.



n channel Enchansment type Mosfet (EMos





n channel EMOSFET ~~consist~~ consist of p type body with two heavily dopped n type material which drain and Source. The Gate terminal is separated by SiO_2 layer

Working of n channel EMOSFET

Case I) When $V_{DS} = +Ve$ and $V_{GS} = 0$ or $V_{DS} = -ve$

If V_{DS} is ↑ then no current will flow because there is no channel i.e. $I_D = 0$

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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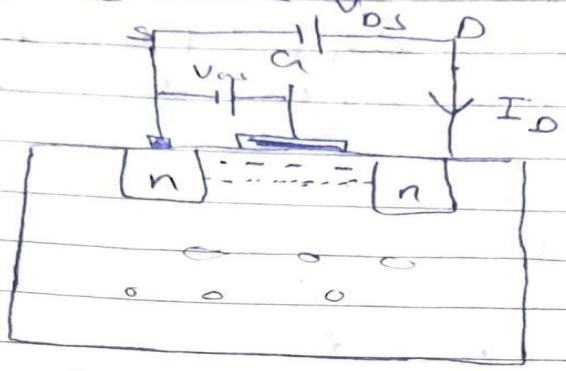
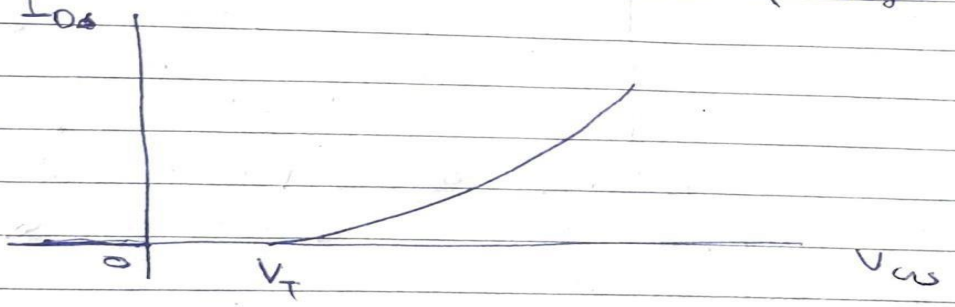
II V_{DS} = +ve, V_{GS} = +ve



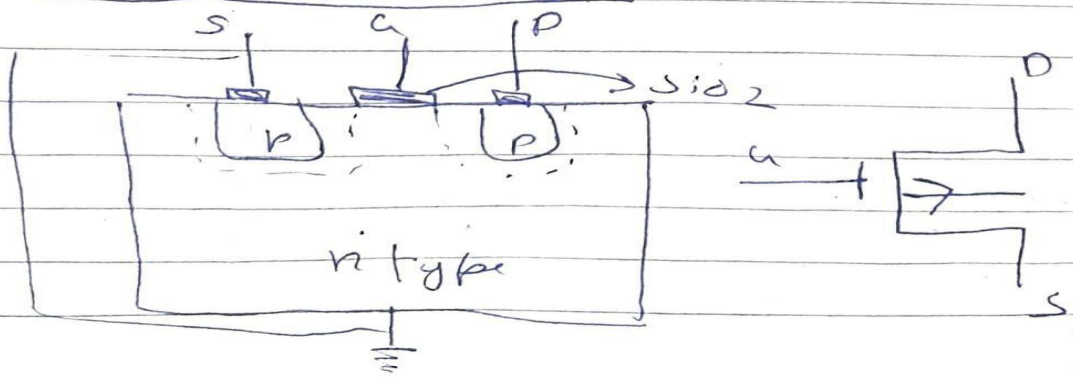
If +ve voltage is applied at gate then e^- in p type move towards the gate and holes moves away from the gate. At that voltage channel is formed is called Threshold voltage (V_T). If V_{GS} is further ↑ed then I_D continuously ↑es.

n channel E MOSFET

Transfer characteristic



P Channel E MOSFET



Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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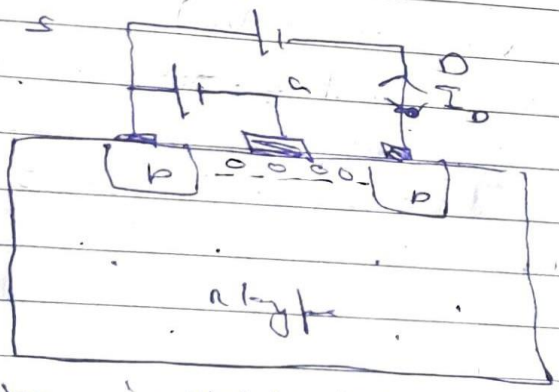
P channel E MOSFET consist of n type body with two heavily dopped p type material which is drain and source. The gate terminal is separated by SiO_2 layer.

Working of P channel E MOSFET

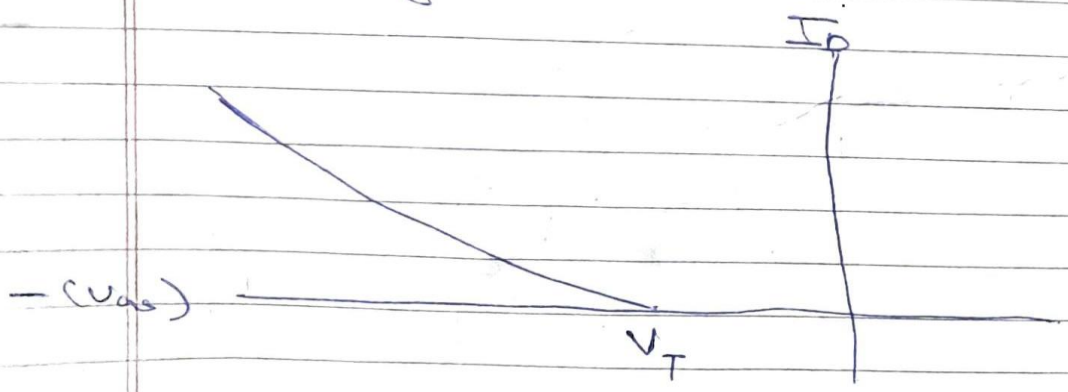
Case I V_{DS} = -ve or +ve $V_{GS} = 0$

If V_{DS} is T there is no current flow because there is no channel is formed

Case II V_{DS} = -ve or V_{GS} = -ve



If -ve voltage is applied to the gate then holes in the n type move towards the gate and e^- move away from the gate.



Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

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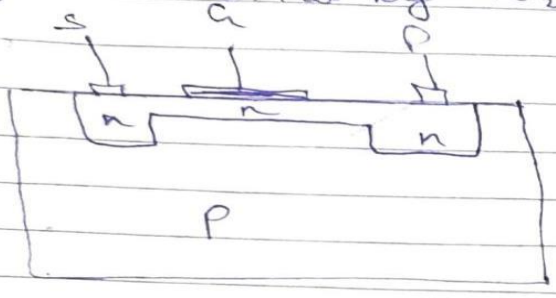
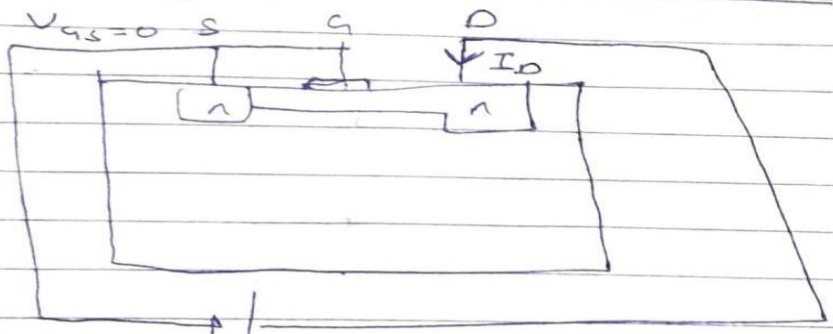
n-Channel Depletion MOSFET (DMOSFET)

n-channel DMOSFET have p type base. Then two n region are formed. A thin layer of SiO_2 is deposited drain and source are connected with metallic contact. An channel is formed b/w two n regions. ~~Gate~~ so I_G is 0. Gate is insulated form n-channel by SiO_2 layer



Working of n channel DMOSFET



Case I $V_{DS} = +V$ $V_{GS} = 0$

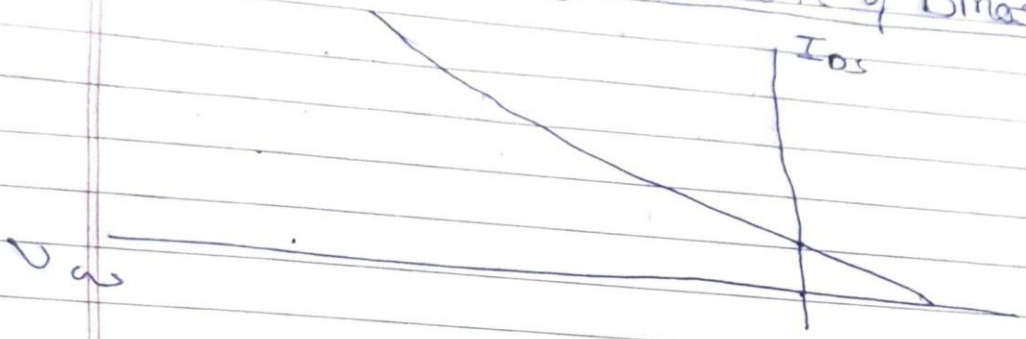
When V_{DS} is ↑ more and more e^- more from S to D so current ↑s A condition comes when current become constant. This condition is called pinch off condition. The value of V_{DS} which established this condition is called pinch off voltage (V_p). After V_p current become constant

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com

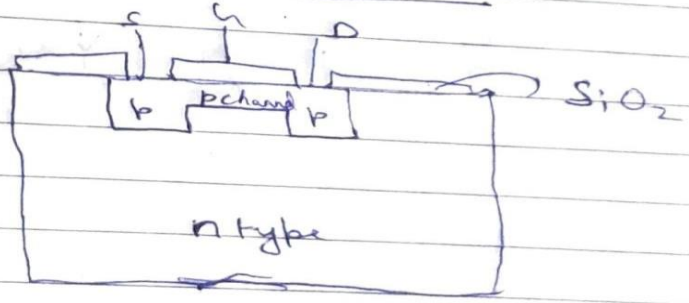
Case II V_{GS} = +ve and V_{DS} = -ve

Id V_{GS} is +ed then holes in p type more towards it. Channel so recombination process occure in channel so pinch off condition comes earlier

Transfer characteristic of DMOSFET



P Channel DMOSFET

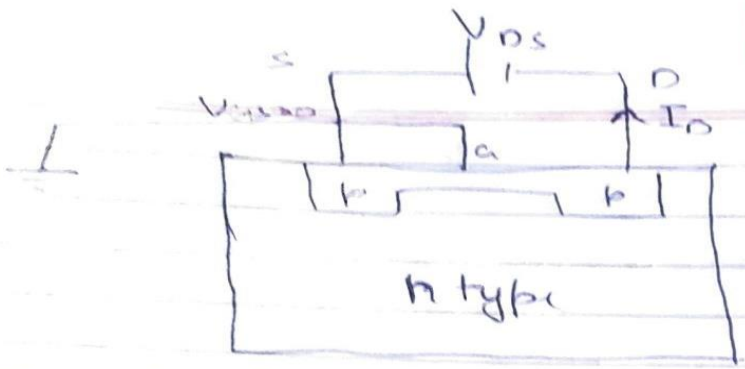


P channel DMOSFET have n type body with two p type region are formed. Drain and Source are connected by metalic contact and gate separated by S_iO_2 layer. A channel is formed b/w two p region.

Working of P channel DMOSFET

Case I V_{GS} = 0 V_{DS} = -ve

Vedansh Agrawal
+91-7088171324
Agrawalvedansh1999@gmail.com



When V_{DS} ↑ more and more holes move from S to D so current ↑es. A condition comes when current becom Constant. This condition is called pinch off condition. At that condition V_{DS} called Pinch off voltage (V_p) After V_p current be come constant

Case II) V_{DS} = -ve and V_{GS} +ve

If V_{GS} is ↑ed than e^- in n type more toward the channel so recombination process occurs in channel so pinch off condition comes earlier.

Vedansh Agrawal
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Agrawalvedansh1999@gmail.com